Figure 1

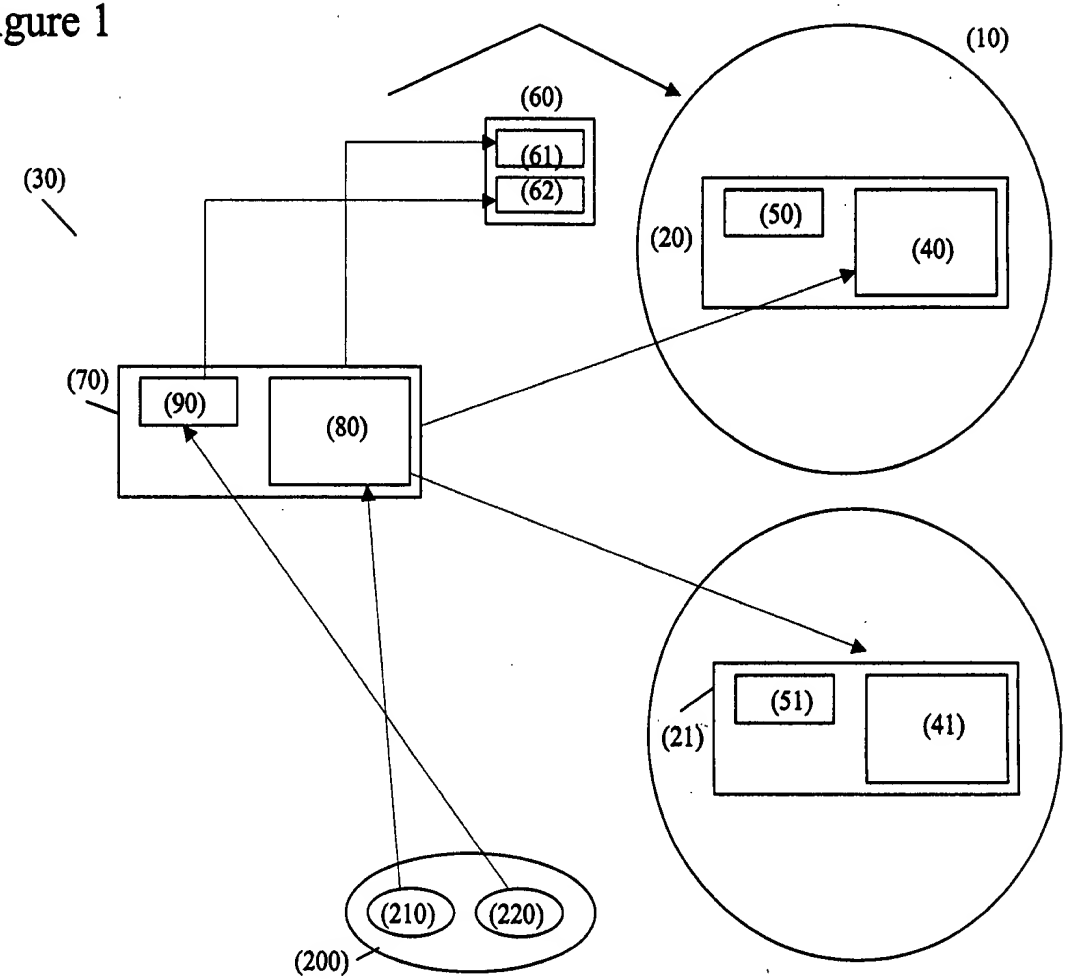
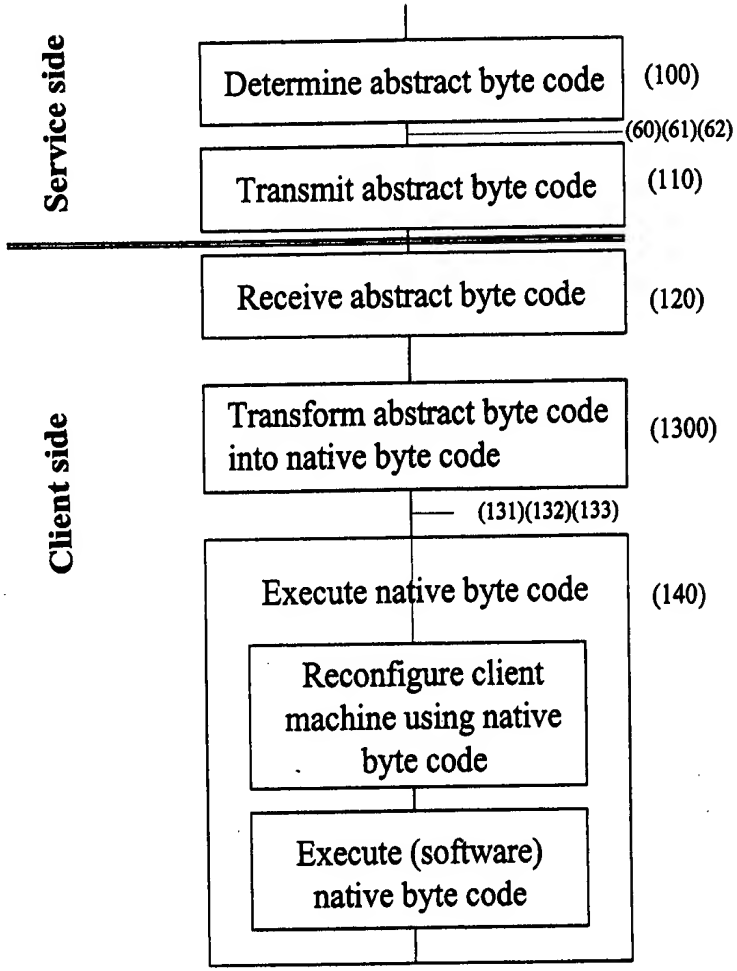


Figure 2


Service side
Determine abstract byte code
(100)
(60)(61)(62)
Transmit abstract byte code
(110)
Receive abstract byte code
(120)
Client side
Transform abstract byte code into native byte code
(1300)
(131)(132)(133)
Execute native byte code
(140)
Reconfigure client machine using native byte code
Execute (software) native byte code

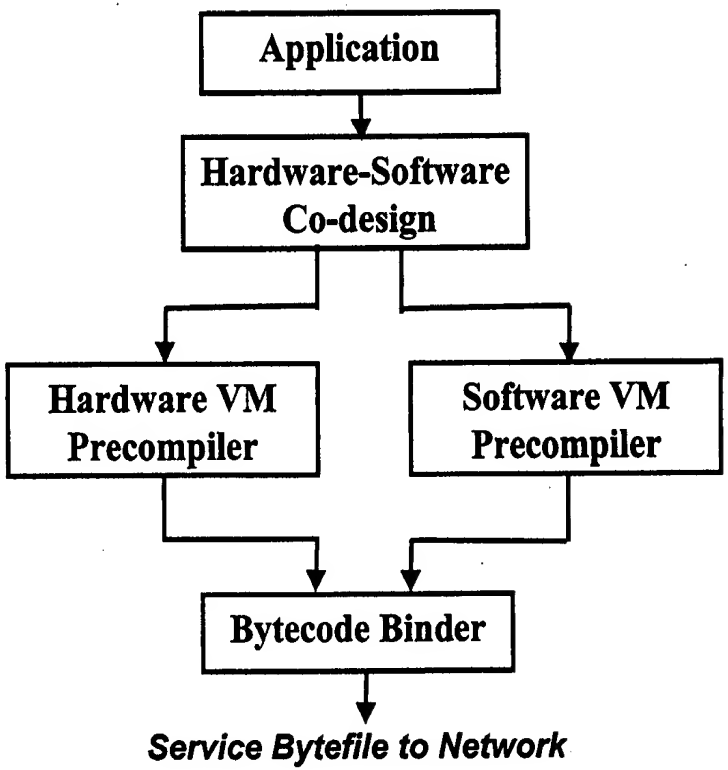

Application
Hardware-Software Co-design
Hardware VM Precompiler
Software VM Precompiler
Bytecode Binder
Service Bytefile to Network

Figure 3

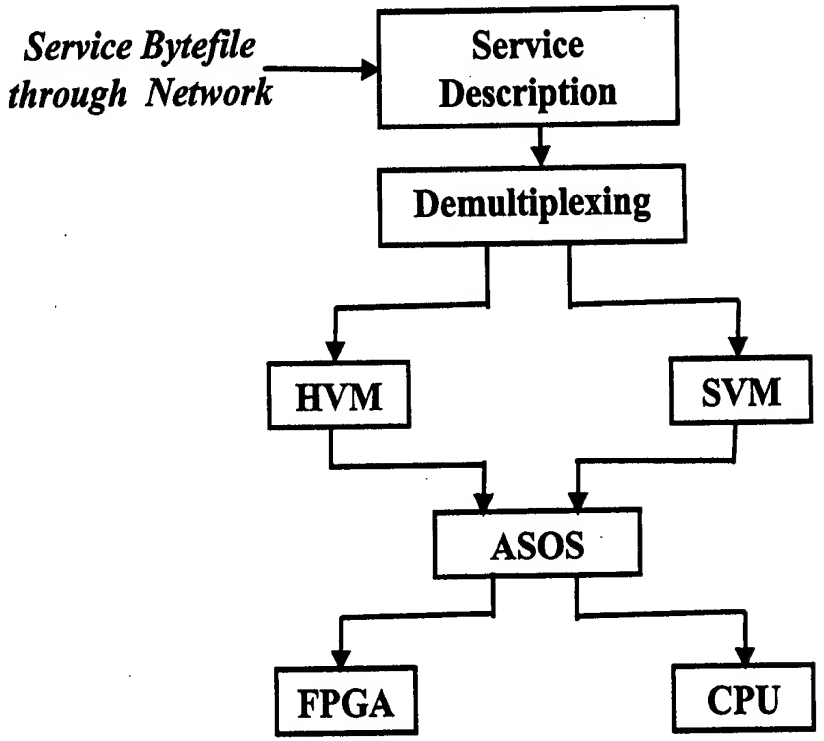


Figure 4

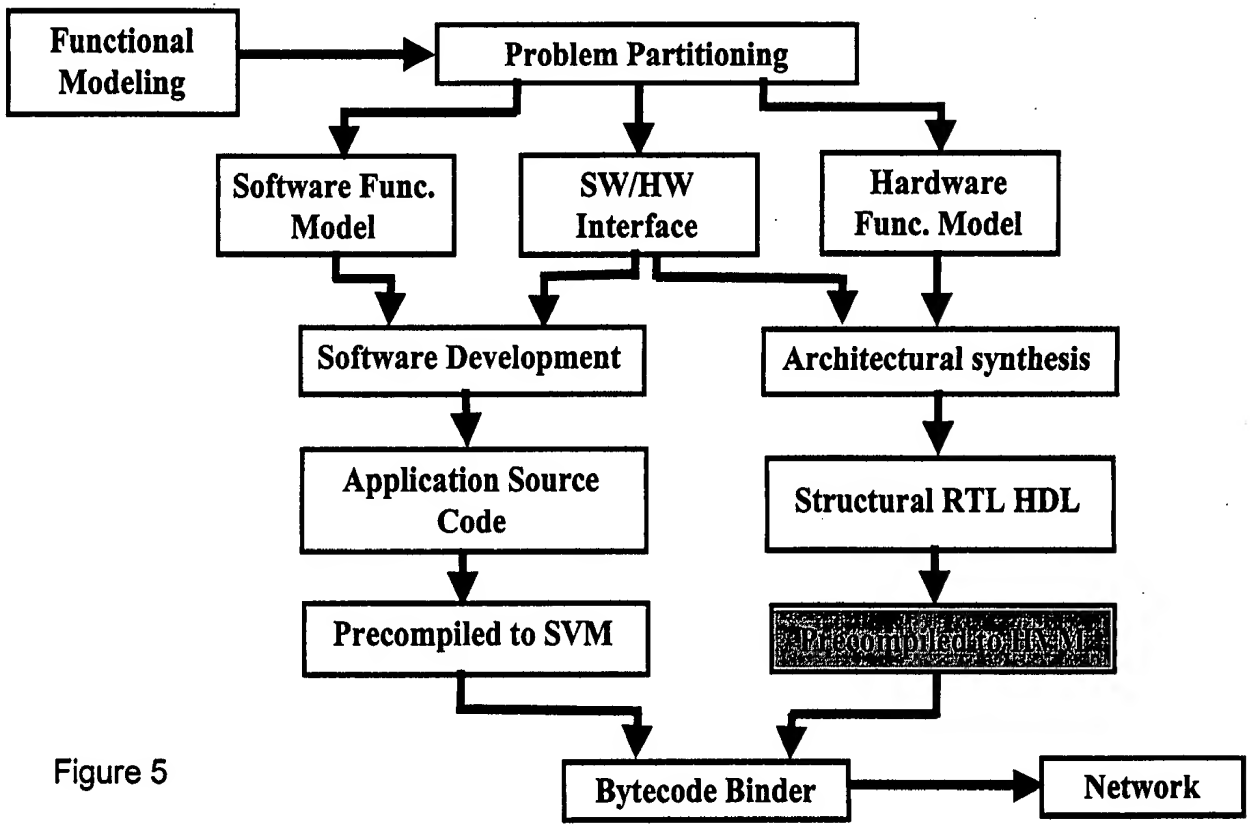


Figure 5

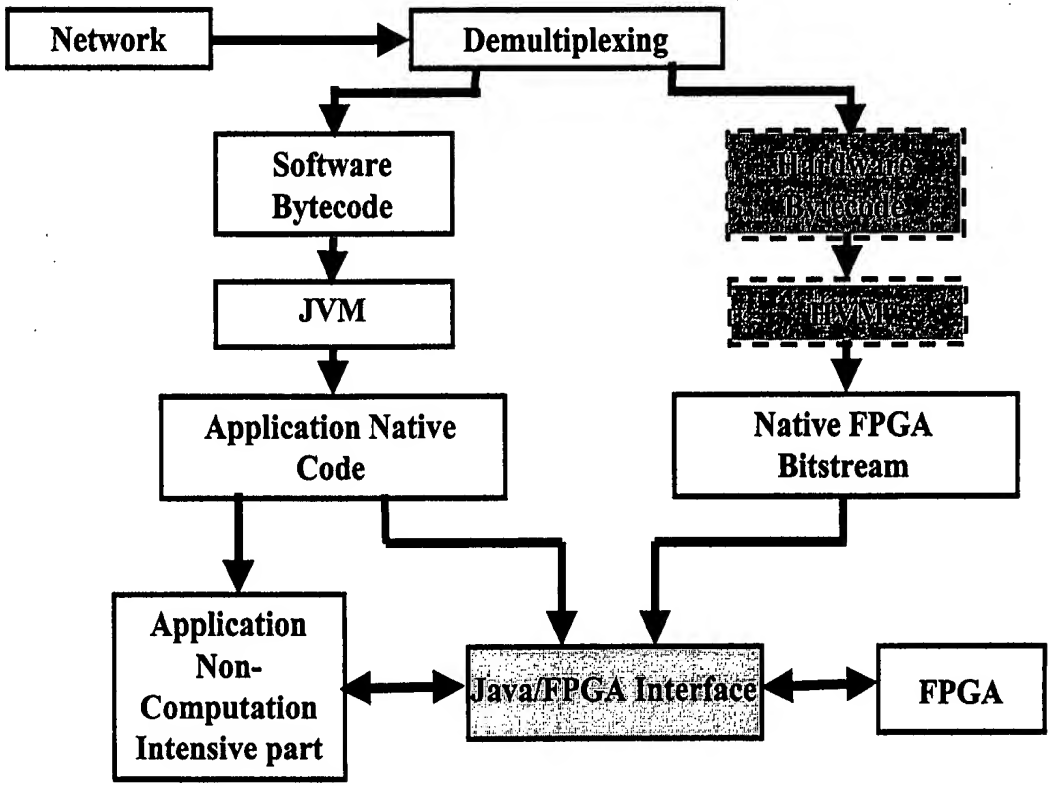

Network
Demultiplexing
Software Bytecode
Hardware Bytecode
JVM
H-VM
Application Native Code
Native FPGA Bitstream
Application Non-Computation Intensive part
Java/FPGA Interface
FPGA

Figure 6

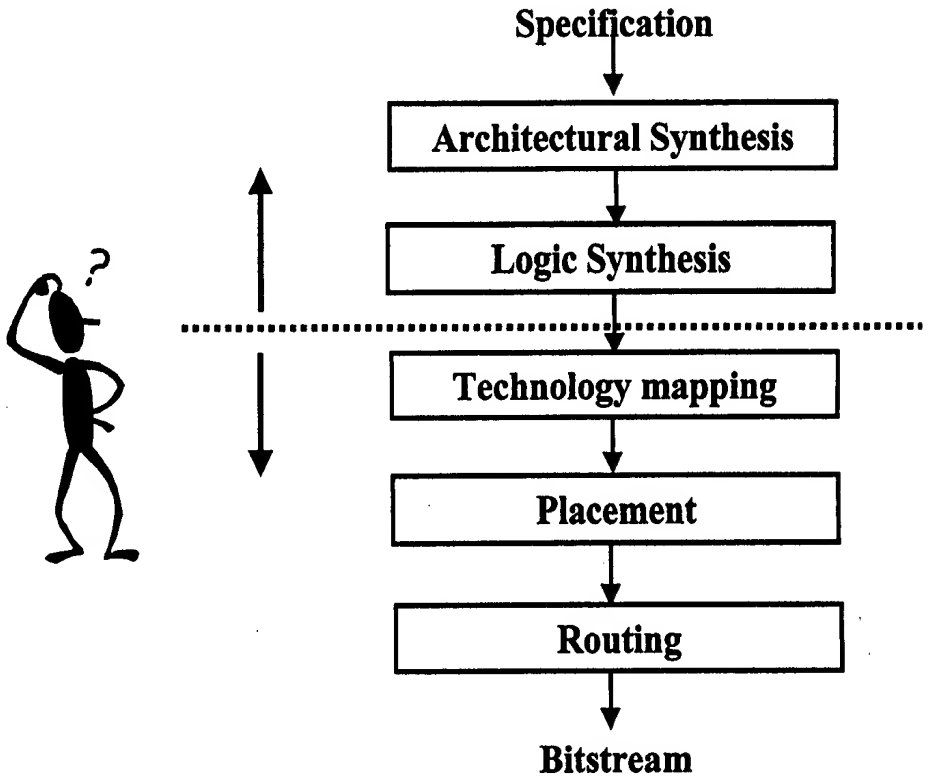

Specification
Architectural Synthesis
Logic Synthesis
Technology mapping
Placement
Routing
Bitstream

Figure 7

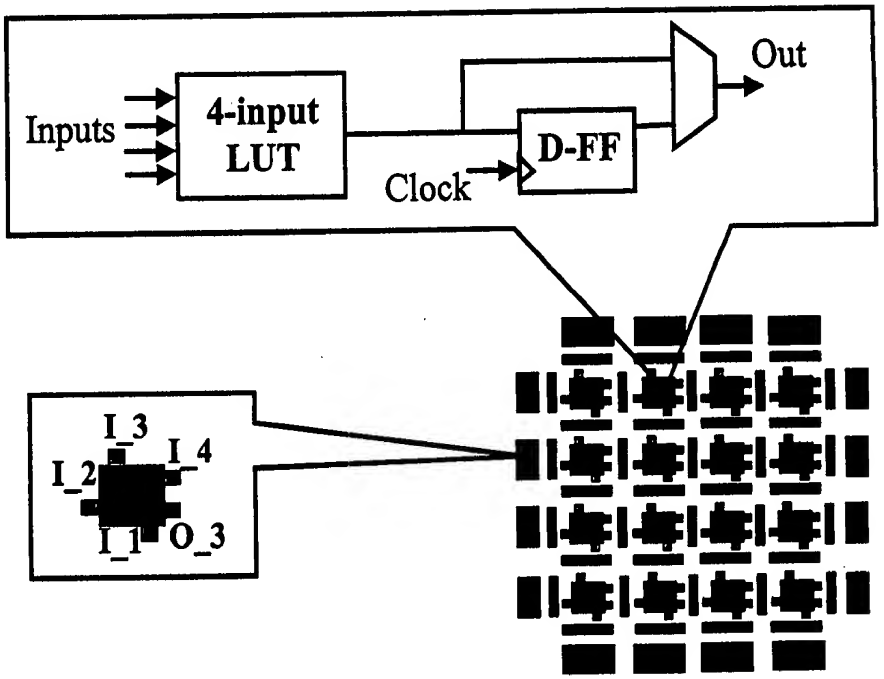


Figure 8

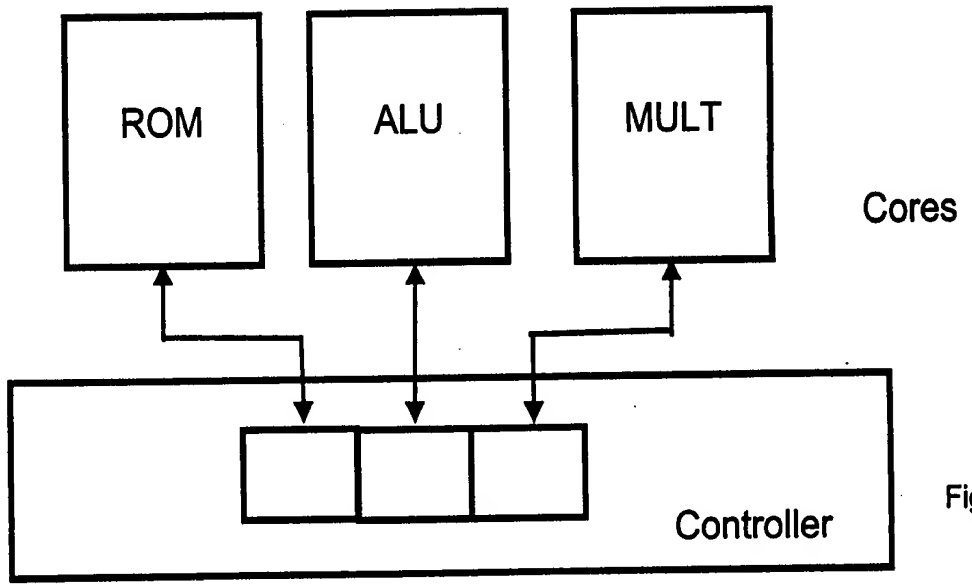


Figure 9

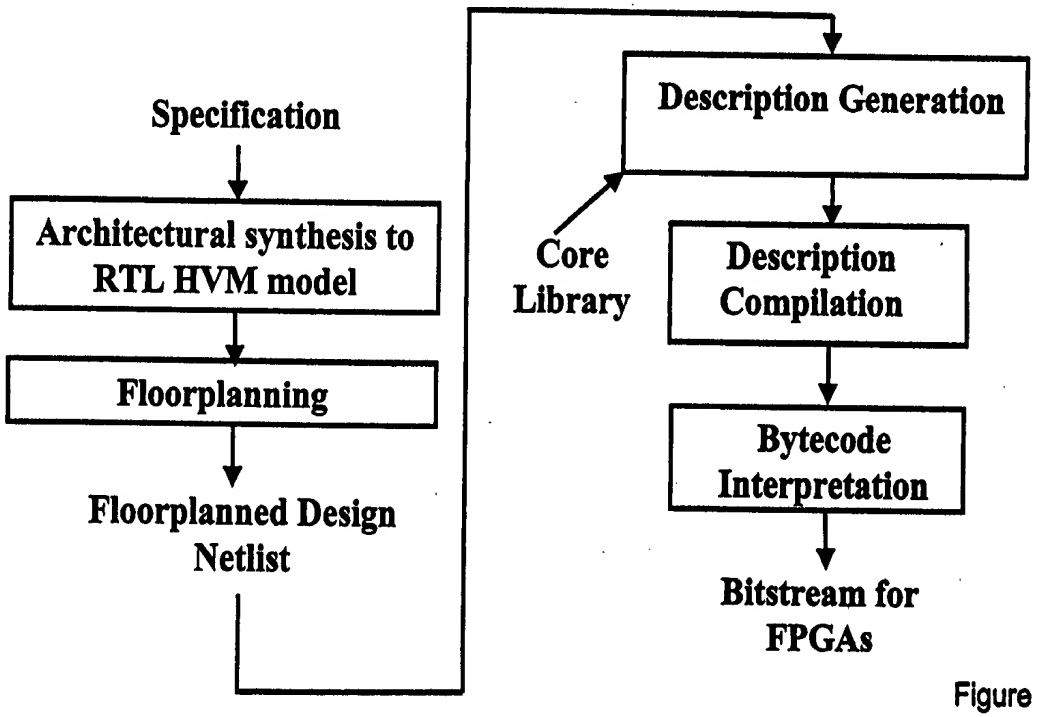

Specification
Architectural synthesis to RTL HVM model
Floorplanning
Floorplanned Design Netlist
Description Generation
Core Library
Description Compilation
Bytecode Interpretation
Bitstream for FPGAs
Service Provider's Side
Client's Side

Figure 10

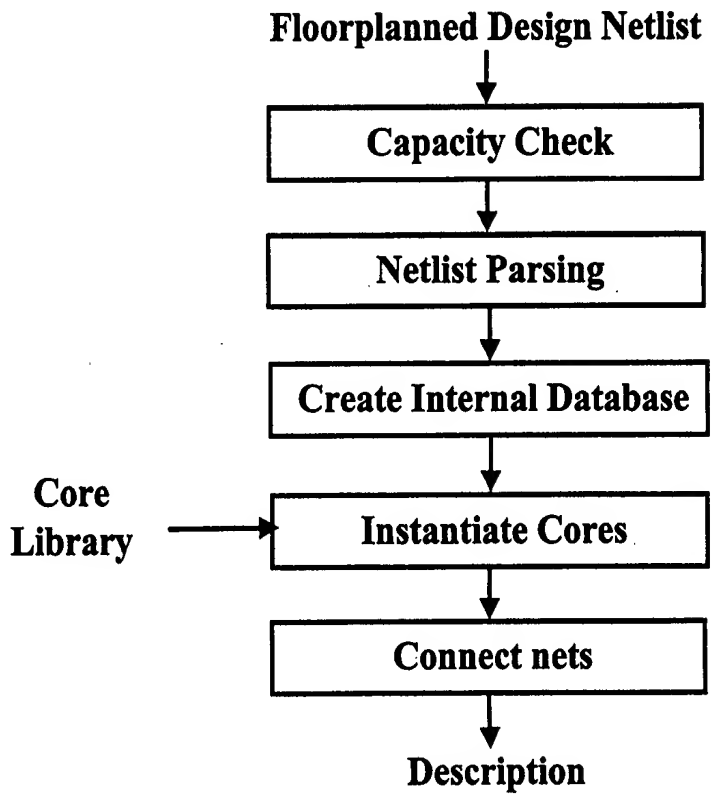

Floorplanned Design Netlist
Capacity Check
Netlist Parsing
Create Internal Database
Core Library
Instantiate Cores
Connect nets
Description

Figure 11

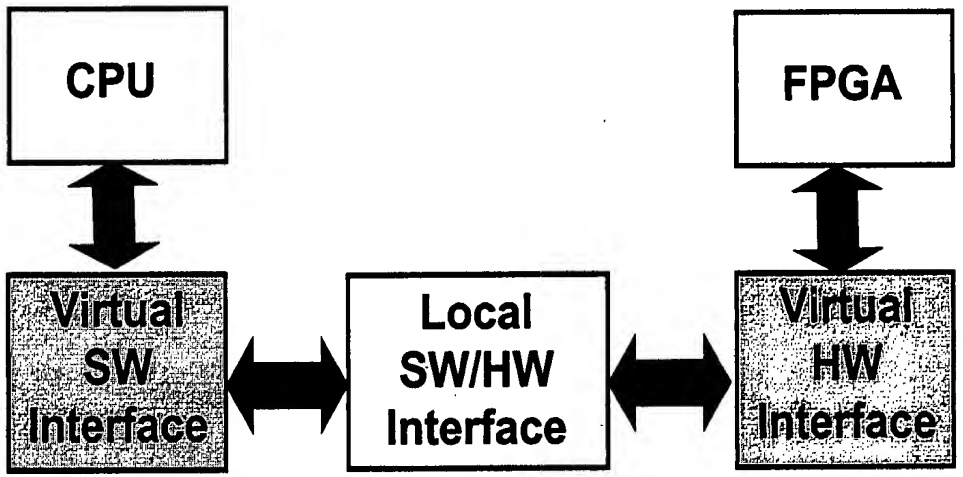

CPU
FPGA
Virtual SW Interface
Local SW/HW Interface
Virtual HW Interface

Figure 12

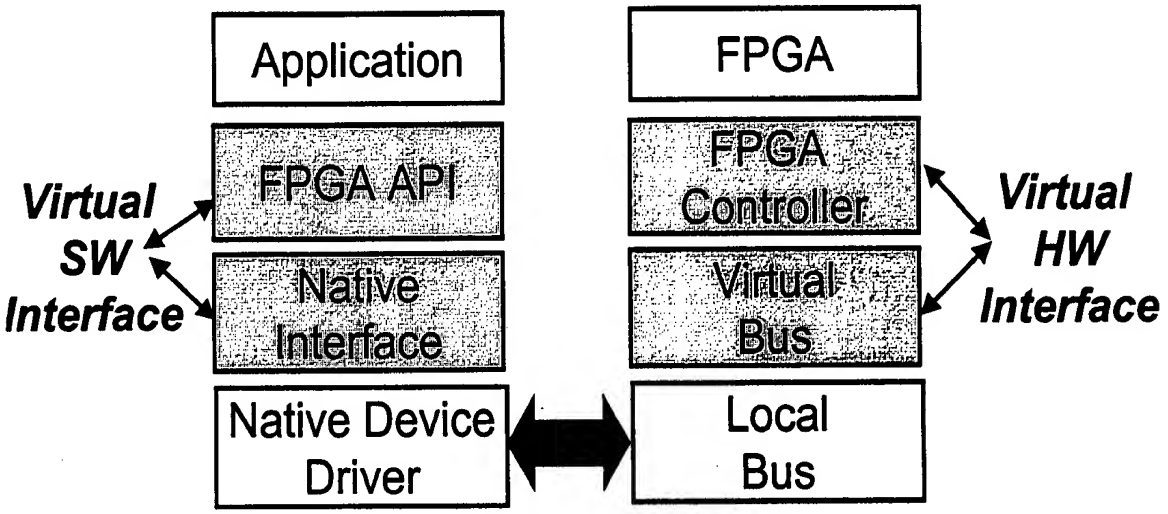

Application
FPGA API
Native Interface
Native Device Driver
Virtual SW Interface
FPGA
FPGA Controller
Virtual Bus
Local Bus
Virtual HW Interface

Figure 13

An Abstract FPGA Model

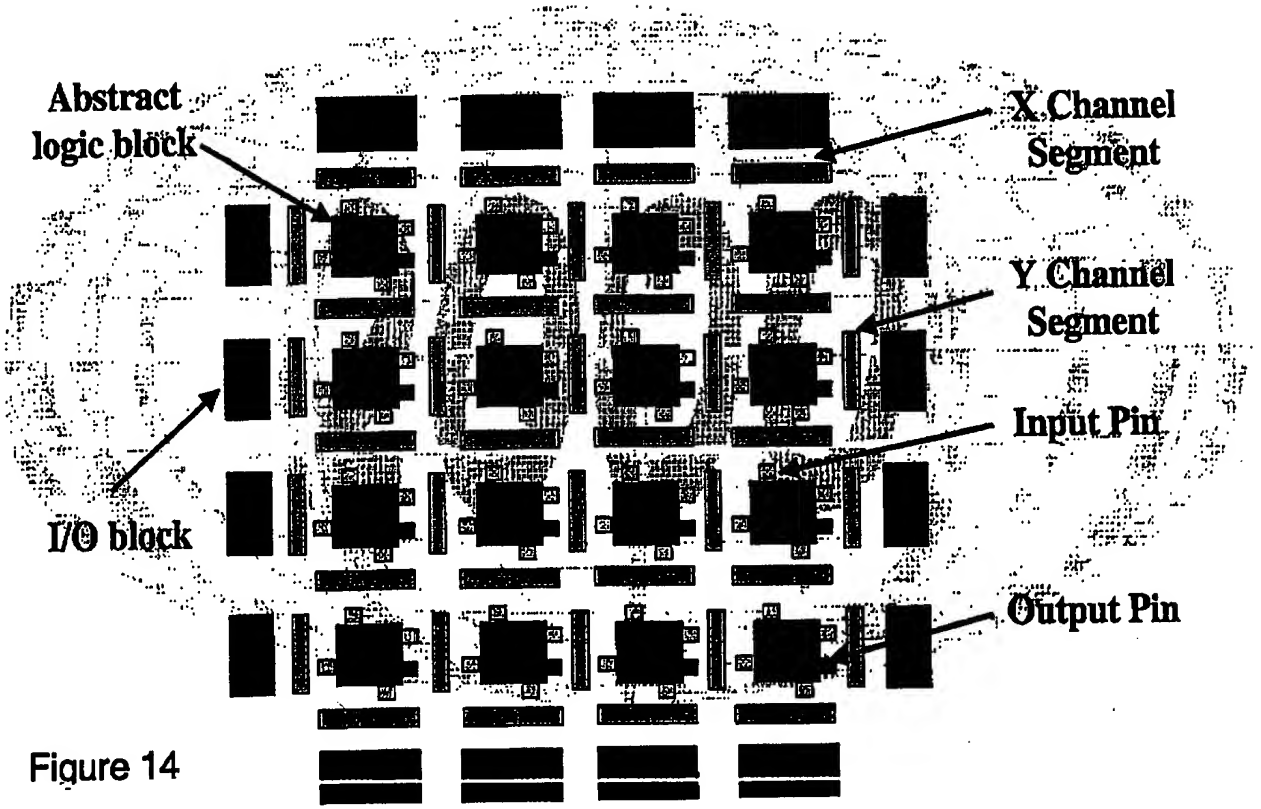


Figure 14